**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancel)
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20. (Original) An information processor, including a decoder for decoding instructions including at least some graphics instructions and at least one paired singles instruction, wherein the decoder is operable to decode a 32-bit paired singles floating point add instruction, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing a pair of 32-bit single-precision floating point values resulting from the paired singles floating point add instruction, bits 11-15 designate a floating point source register storing a pair of 32-bit single-precision floating point values, bits 16-20 designate a further floating point source register storing a pair of 32-bit single-precision floating point values, bits 21-25 encode a reserved field of "00000", bits 26-30 encode a secondary op code of 21, and bit 31 comprises a record bit indicating updating of a condition register.

21. (Original) An information processor, including a decoder for decoding instructions including at least some graphics instructions and at least one paired singles instruction, wherein the decoder is operable to decode a 32-bit paired-single-scalar-vector-multiply-add-high (ps_madds0x) instruction wherein a high order word of a paired singles register is used as a scalar, and further wherein the ps_madds0x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 14 and bit 31 comprises a record bit indicating updating of a condition register.

22. (Original) The information processor, including a decoder for decoding instructions including at least some graphics instructions and at least one paired singles instruction, wherein the decoder is operable to decode a 32-bit paired-single-scalar-vector-multiply-add-low (ps_madds1x) instruction wherein a low order word of a paired singles register is used as a scalar, and further wherein the ps_madds1x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 15 and bit 31 comprises a record bit indicating updating of a condition register.

23. (Cancel)

24. (Original) A decoder for decoding instructions including at least some graphics instructions, wherein the decoder is operable to decode:

a 32-bit paired singles floating point add instruction, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing a pair of 32-bit single-precision floating point values resulting from the paired singles floating point add instruction, bits 11-15 designate a floating point source register storing a pair of 32-bit single-precision floating point

values, bits 16-20 designate a further floating point source register storing a pair of 32-bit single-precision floating point values, bits 21-25 encode a reserved field of "00000", bits 26-30 encode a secondary op code of 21, and bit 31 comprises a record bit indicating updating of a condition register;

a 32-bit paired-single-scalar-vector-multiply-add-high (ps_madds0x) instruction wherein a high order word of a paired singles register is used as a scalar, and further wherein the ps_madds0x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 14 and bit 31 comprises a record bit indicating updating of a condition register; and

a 32-bit paired-single-scalar-vector-multiply-add-low (ps_madds1x) instruction wherein a low order word of a paired singles register is used as a scalar, and further wherein the ps_madds1x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 15 and bit 31 comprises a record bit indicating updating of a condition register.

25. (Original) A storage medium storing a plurality of instructions including at least some graphics instructions and a 32-bit paired singles floating point add instruction, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing a pair of 32-bit single-precision floating point values resulting from the paired singles floating point add instruction, bits 11-15 designate a floating point source register storing a pair of 32-bit single-precision floating point values, bits 16-20 designate a further floating point source register storing a pair of 32-bit single-precision floating point values, bits 21-25 encode a reserved field of "00000", bits 26-30 encode a secondary op code of 21, and bit 31 comprises a record bit indicating updating of a condition register.

26. (Original) A storage medium storing a plurality of instructions including at least some graphics instructions and a 32-bit paired-single-scalar-vector-multiply-add-high (ps_madds0x) instruction wherein a high order word of a paired singles register is used as a scalar, and further wherein the ps_madds0x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 14 and bit 31 comprises a record bit indicating updating of a condition register.

27. (Original) A storage medium storing a plurality of instructions including at least some graphics instructions and a 32-bit paired-single-scalar-vector-multiply-add-low (ps_madds1x) instruction wherein a low order word of a paired singles register is used as a scalar, and further wherein the ps_madds1x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 15 and bit 31 comprises a record bit indicating updating of a condition register.

28. (Original) A storage medium storing a plurality of instructions including at least some graphics instructions and:

a 32-bit paired singles floating point add instruction, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing a pair of 32-bit single-precision floating point values resulting from the paired singles floating point add instruction, bits 11-15 designate a floating point source register storing a pair of 32-bit single-precision floating point values, bits 16-20 designate a further floating point source register storing a pair of 32-bit single-precision floating point values, bits 21-25 encode a reserved field of "00000", bits 26-30 encode a secondary op code of 21, and bit 31 comprises a record bit indicating updating of a condition register;

a 32-bit paired-single-scalar-vector-multiply-add-high (ps_madds0x) instruction wherein a high order word of a paired singles register is used as a scalar, and further wherein the ps_madds0x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for

storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 14 and bit 31 comprises a record bit indicating updating of a condition register; and

a 32-bit paired-single-scalar-vector-multiply-add-low (ps_madds1x) instruction wherein a low order word of a paired singles register is used as a scalar, and further wherein the ps_madds1x instruction includes bits 0 through 31, wherein bits 0-5 encode a primary op code of 4, bits 6-10 designate a floating point destination register for storing the results of the instruction, bits 11-15 designate a first floating point register as a first source storing a first pair of 32-bit single-precision floating point values, bits 16-20 designate a second floating point register as a second source storing a second pair of 32-bit single-precision floating point values, bits 21-25 designate a third floating point register as a third source storing a third pair of 32-bit single-precision floating point values, bits 26-30 encode a secondary op code of 15 and bit 31 comprises a record bit indicating updating of a condition register.